CLAIMS

What is claimed is:

1. A method for semiconductor device feature development using a bi-layer photoresist comprising the steps of:

providing a non-silicon containing photoresist layer over a substrate;

providing a silicon containing photoresist over the non-silicon containing photoresist layer;

exposing said silicon containing photoresist layer to an activating light source an exposure surface defined by an overlying pattern according to a photolithographic process;

developing said silicon containing photoresist layer according to a photolithographic process to reveal a portion the non-silicon containing photoresist layer; and

dry developing said non-silicon containing photoresist layer in a plasma reactor by igniting a plasma from an ambient mixture including at least oxygen, carbon monoxide, and argon.

2. The method of claim 1, wherein the plasma reactor includes at least one RF power source for plasma excitation and at least one RF power source for accelerating plasma generated ions towards the substrate surface.

3. The method of claim 1, wherein the non-silicon containing photoresist layer comprises a non-photoactive polymer.

4. The method of claim 1, wherein the ambient mixture includes about 1 part oxygen, about 10 to about 50 parts carbon monoxide, and about 10 to about 50 parts Argon.

5. The method of claim 1, wherein the activating light source has a wavelength of one of about 157 nanometers and about 193 nanometers.

6. The method of claim 1, wherein the non-silicon containing photoresist layer has a thickness greater than the silicon containing photoresist layer.

7. The method of claim 6, wherein the non-silicon containing photoresist layer has a thickness of about 1000 Angstroms to about 5000 Angstroms and the silicon containing photoresist layer has a thickness of about 500 Angstroms to about 3000 Angstroms.

8. The method of claim 2, further comprising the step of removing the silicon containing photoresist layer according to a first in-situ ashing process.

9. The method of claim 8, wherein the first in-situ ashing process includes igniting a plasma to include nitrogen, fluorine, and oxygen ions.

10. The method of claim 8, further comprising the step of etching a semiconductor feature according to a reactive ion etch process.

11. The method of claim 10, wherein the semiconductor feature includes one of a via hole, a trench line, a contact hole, a shallow trench isolation feature, and a polysilicon gate feature.

12. The method of claim 10, wherein the reactive ion etch process includes hydrofluorocarbon containing ambient having a fluorine to carbon ratio of at most about 2.

13. The method of claim 10, further comprising the step of removing the non-silicon containing photoresist layer according to a second in-situ ashing process.

14. The method of claim 13, wherein the second in-situ ashing process includes igniting a plasma to include nitrogen, fluorine, and oxygen ions, said plasma optimized to simultaneously clean plasma contact surfaces.

15. The method of claim 14, wherein the plasma operating conditions include maintaining an ambient pressure of about 5 to about 20 mTorr, supplying power to the first RF power source at about 200 to about 300 Watts, and supplying power to the second RF power source at about 100 to about 150 Watts.

16. The method of claim 14, further comprising the step of reactively ion etching through a thickness of a metal nitride layer using a hydrofluorocarbon containing plasma to at least partially form the semiconductor feature including one of a via hole and contact hole.

17. The method of claim 16, further comprising the step of performing an in-situ cleaning process including igniting a plasma to include nitrogen, fluorine, and oxygen ions, said plasma optimized to clean plasma contact surfaces.

18. The method of claim 17, wherein the plasma operating conditions include maintaining an ambient pressure of about 5 to about 20 mTorr, supplying power to the first RF power source at about 200 to about 300 Watts, and supplying power to the second RF power source at about 100 to about 150 Watts.

19. The method of claim 17, wherein the step including the first in-situ ashing process is combined with the step including the second in-situ ashing process to reduce a sequential number of steps.